LOW-LATENCY EQUALIZATION IN MULTI-LEVEL, MULTI-LINE COMMUNICATION SYSTEMS

5   ## Background

The present invention relates to multi-level digital signaling, and in particular to techniques to equalize or compensate for errors that may otherwise be present in a multi-level, multi-line signaling system.

10   The use of multiple signal levels instead of binary signal levels is a known technique for increasing the data rate of a digital signaling system, without necessarily increasing the signal frequency of the system. Such multi-level signaling is sometimes known as multiple pulse

15   amplitude modulation or multi-PAM, and has been implemented with radio or other long-distance wireless signaling systems.

Other long-distance uses for multi-PAM signaling include computer or telecommunication systems that employ

20   Gigabit Ethernet over optical fiber (IEEE 802.3z) and over copper wires (IEEE 802.3ab), which use three and five signal levels, respectively, spaced symmetrically about and including ground. Equalization techniques for long-distance multi-level signaling systems such as those used

25   in radio or telecommunication networks commonly include adaptive filters, which can change equalization characteristics adaptively to improve equalization accuracy or in response to changing conditions. The complexities of these equalization techniques can delay signaling by slight

30   but tolerable amounts for these long-distance systems.

Multi-PAM is not traditionally used for communication between devices in close proximity or belonging to the same system, such as those connected to the same integrated

circuit (IC) or printed circuit board (PCB). One reason
for this may be that within such a system the
characteristics of transmission lines, such as buses or
signal lines, over which signals travel are tightly
5   controlled, so that increases in data rate may be achieved
by simply increasing data frequency. At higher
frequencies, however, receiving devices may have a reduced
ability to distinguish binary signals, so that dividing
signals into smaller levels for multi-PAM is problematic.
10 Multi-PAM may also be more difficult to implement in multi-
drop bus systems (i.e., buses shared by multiple processing
mechanisms), since the lower signal-to-noise ratio for such
systems sometimes results in bit errors even for binary
signals. Moreover, complex equalization techniques such as
15 employed for long distance communication systems may not be
feasible in a bus system for which low latency is a
performance criterion.

Summary

20   The present invention is directed to low-latency
equalization mechanisms for short-range communications
systems. Such equalization mechanisms may compensate for
signal attenuation along a transmission line, reflections
due to impedance discontinuities along such a line, and
25 crosstalk between adjacent lines. The equalization
mechanisms may be particularly advantageous for multi-PAM
communications systems.

Brief Description of the Figures

30   FIG. 1 shows a multi-level signaling system having
four logical states corresponding to four voltage ranges.

FIG. 2 shows a representative signaling device that may be used to create the voltage levels of FIG. 1.

FIG. 3 depicts an issue with a multi-PAM signaling system such as the 4-PAM system shown in FIG. 1 and FIG. 2.

5   FIG. 4 shows a solution to the issue depicted in FIG. 3.

FIG. 5 depicts a multi-level (4-PAM) signaling system in which voltage ranges for the logic states are shifted by varying amounts to implement the solution shown in FIG. 4.

10   FIG. 6 provides a table illustrating the signal levels involved in transitioning between the logical states of FIG. 5.

FIG. 7A shows initial, transition and final states of a signal that may represent a transition illustrated in

15   FIG. 6.

FIG. 7B shows initial, transition and final states of a main component of the signal shown in FIG. 7A.

FIG. 7C shows initial, transition and final states of an auxiliary component of the signal shown in FIG. 7A.

20   FIG. 8 shows a device that can provide the transition signals shown in FIG. 6 and FIGs. 7A-C.

FIG. 9 shows a finite impulse response (FIR) filter representation of the device of FIG. 8.

FIG. 10 shows a general equalization system for a

25   signal line, including a self equalization FIR filter and a number of crosstalk equalization FIRs.

FIG. 11A shows a signal transition that may create crosstalk on adjacent signal lines.

FIG. 11B shows crosstalk noise from the signal

30   transition of FIG. 11A, imposed on a signal in an adjacent line.

FIG. 11C shows an equalization signal that compensates for the crosstalk noise shown in FIG. 11B.

FIG. 11D shows a first component of the equalization signal shown in FIG. 11C.

5 FIG. 11E shows a second component of the equalization signal shown in FIG. 11C.

FIG. 12 shows a signal driver, self-equalization and crosstalk equalization communication device.

FIG. 13 shows an equalization mechanism that inputs 10 MSB and LSB signals to provide compensation.

FIG. 14 shows a general FIR filter having a number of self-equalization and crosstalk-equalization mechanisms tapped at various delay times.

FIG. 15 illustrates a mechanism for adjusting 15 equalization parameters such as the magnitude, timing and sign of various equalization signals.

FIG. 16 shows an encoder that converts MSB and LSB signals into input signals for the output driver and equalization mechanisms.

20 FIG. 17 shows receiver that receives the multi-level signals sent by the main and auxiliary drivers and decode the signals into MSB and LSB components.

FIG. 18A shows a signal transition that has a high-frequency noise spike.

25 FIG. 18B shows an equalization signal designed to compensate for a DC component of the spike of FIG. 18A. *and Fig.18b*
~~FIG. 18C shows a smoothing of the signal of FIG. 17B~~ by integration.

FIG. 19 shows a system with a number of adjacent 30 signal lines that may create crosstalk, and standardized FIR filters coupled between the lines.

FIG. 20 shows a system with a number of adjacent signal lines grouped in pairs with a ground wire disposed between the pairs of lines and standardized FIR filters coupled between the lines.

FIG. 21 illustrates a memory system in which embodiments of the present invention may be applied.

Detailed Description of the Preferred Embodiment

FIG. 1 shows a multi-level signaling system having four logical states corresponding to four voltage levels, VOUT0, VOUT1, VOUT2 and VOUT3. The voltage levels in this example are all positive relative to ground, and range as high as VTERM. VOUT0 is defined to be above VREFH, VOUT1 is defined to be between VREFM and VREFH, VOUT2 is defined to be between VREFL and VREFM, and VOUT3 is defined to be less than VREFL. VOUT0 corresponds to logical state 00, VOUT1 corresponds to logical state 01, VOUT2 corresponds to logical state 11, and VOUT3 corresponds to logical state 10. A first bit of each logical state is termed the most significant bit (MSB) and a second bit of each logical state is termed the least significant bit (LSB). Each logical state may be termed a dual-bit, since it provides information regarding two bits. Data may be transmitted and read at both rising and falling edge of a clock cycle, so that each bit signal and each dual-bit signal has a duration of one-half the clock cycle. The logical states are arranged in a Gray coded order, so that an erroneous reading of an adjacent logic state produces an error in only one of the bits. Another characteristic of this logical 4-PAM arrangement is that setting the LSB equal to zero for all states results in a 2-PAM scheme.

Alternatively, the logical states can be arranged in binary (00, 01, 10, 11) or other order.

In one embodiment the communication system is employed for a memory bus, which may for instance include random
5   access memory (RAM), like that disclosed in U.S. Patent Number 5,243,703 to Farmwald et al., which is incorporated herein by reference. The multi-PAM communication and low-latency signal correction techniques disclosed herein may also be used for other contained systems, such as for
10 communication between processors of a multiprocessor apparatus, or between a processor and a peripheral device, such as a disk drive controller or network interface card over an input/output bus.

FIG. 2 shows a representation of a communication
15 system that may be used to create the voltage levels of FIG. 1. An output driver 20 drives signals to output pad 18 and over transmission line 16, which may for example be a memory bus or other interconnection between devices affixed to a circuit board, to be received at pad 25.
20 Transmission line 16 has a characteristic impedance Z_0 27 that is substantially matched with a terminating resistor 29 to minimize reflections. Output driver 20 includes first 21, second 22 and third 23 transistor current sources, which together produce a current I when all are
25 active, pulling the voltage at pad 25 down from VTERM by $I \cdot Z_0$, signaling logical state 10 under the Gray code system. To produce voltage VOUT0=VTERM, signaling logical state 00, current sources 21, 22 and 23 are all turned off. To produce voltage VOUT1=VTERM-$(1/3)I \cdot Z_0$, signaling logical
30 state 01, one of the current sources is turned on, and to produce voltage VOUT2=VTERM-$(2/3)I \cdot Z_0$, two of the current sources are turned on. The logical level 00 is chosen to

have zero current flow to reduce power consumption for the situation in which much of the data transmitted has a MSB and LSB of zero. The reference levels are set halfway between the signal levels, so that $VREFH=VTERM-(1/6) \ I \cdot Z_0$,

5     $VREFM=VTERM-(1/2) \ I \cdot Z_0$ and $VREFL=VTERM(5/6) \ I \cdot Z_0$. Related disclosure of a multi-PAM signaling system can be found in U.S. Patent Application Serial Number 09/478,916, entitled Low Latency Multi-level Communication Interface, filed on January 6, 2000, which is incorporated by reference herein.

10   Also incorporated by reference herein is a Provisional U.S. Patent Application entitled, "A 2Gb/s/pin 4-PAM parallel bus interface with transmit crosstalk cancellation & equalization and integrating receivers," filed on even date herewith, by Express Mail Label No.EK533218494US, inventors

15   Pak Shing Chau et al.

FIG. 3 depicts an issue with a multi-PAM signaling system such as the 4-PAM system mentioned above. For cases in which attenuation of a signal exists between transmission and reception, different amounts of signal

20   loss may occur depending upon the magnitude of the transition between logic levels. For instance, transitioning between a 10 state and a 00 state may have a greater signal deficiency than a transition between a 11 state and the 00 state, which in turn has a greater signal

25   deficiency than a transition between 01 state and the 00 state, while maintaining the same logic state over plural bit periods may have no attenuation error. Thus each different transition between states may have a different associated error. Complicating matters is the transitory

30   nature of the errors as demonstrated, for example, by the fact that maintaining a constant logic state may generate no error, regardless of the previous transition magnitude

to that logic state and the error associated with that transition.

FIG. 4 shows the addition of a different equalization signal, 3S, 2S or S to the main signal when driving

5 different transitions, the equalization signals compensating for the attenuation of the received signal. The equalization signals in this embodiment are transitory, so that each may for instance have a duration less than or equal to one bit signal, after which the equalization

10 signal is terminated, allowing the initially overdriven signal to maintain a steady state logic level. Stated differently, the equalization signals S, 2S or 3S add predetermined high-frequency components to the transition signals that raise the slope of the edge of the transition.

15 A difficulty with this approach for a system such as shown in FIG. 1 is that the voltage can only be pulled down from VTERM, unless negative current could flow through current sources 21-23. In other words, with the 00 level set at VTERM in FIG. 5 it is difficult for the equalizing S, 2S or

20 3S to add to the transition above VTERM.

FIG. 5 depicts a multi-level (4-PAM) signaling system in which the 00 logic state is reduced below VTERM by 3S, in order to allow overdriving a transition for example from the 10 to the 00 state by 3S. This 00 logic level is

25 termed A, and can be provided by having none of the main current drivers turned on and three equalization drivers turned on, for a voltage level of 0M+3S. On the other hand, the 10 level (termed D) can be pulled lower if necessary to overdrive a transition, and so it is

30 characterized by having three main drivers or current sources turned on, but zero equalization drivers turned on, for a total voltage level of 3M+0S. Logical state 01, also

termed level B, has a voltage of 1M+2S, while state 11, termed level C, has a voltage of 2M+1S. The reference levels that provide boundaries between the signal levels are also shifted in accordance with the shift in the signal

5　levels. Thus VRH is defined in this system to be equal to VTERM-$(1/2)[(1/3)+(5/3)(S/M)]I \cdot Z_0$, VRM is defined in this system to be equal to VTERM-$(1/2)[1+(S/M)]I \cdot Z_0$ and VRL is defined in this system to be equal to VTERM-$(1/2)[(5/3)+ (1/3)(S/M)]I \cdot Z_0$.

10　　　FIG. 6 provides a table illustrating the drive signal levels involved in transitioning between the logical states of FIG. 5. In order to transition from initial state A (0M+3S) to final state D (3M+0S), for example, an overdriven transition drive signal of 3M+3S is provided.

15　Conversely, changing from an initial state D (3M+0S) to final state A (0M+3S) involves a drive signal of 0M+0S. The transition drive signal in this example has an overdriven duration that is equal to that of one bit (or dual-bit) signal, although in general an overdriven period

20　of a drive signal may have a duration that is less than or greater than that of a bit signal. For example, a drive signal may be overdriven for a first portion of a bit signal time, with a second portion of that signal not being overdriven.

25　　　Several characteristics are apparent from the table of FIG. 6. First note that for the received signals, the M multiplier is the complement of the S multiplier. Also note that the drive signal S multiplier is equal to the initial S multiplier, while the transition M multiplier is

30　equal to the final M multiplier. Also note that the table depicted in FIG. 6 illustrates just one set of transition drive signals specific to a 4-PAM signaling system with a

single error correction, and may be extrapolated to be used with communication systems having additional signal levels and additional error corrections. For instance, a similar table may be constructed to deal with signal reflections,

5 although such reflections may be either positive or negative and may have a delay of more than one bit signal duration, as measured at the signal receiver.

FIG. 7A-C show drive signals that may, for example, represent the transition from state D to A of FIG. 6, which

10 for clarity of illustration is then shown to remain at state A for the next bit signal. FIG. 7A shows a signal 50 with an overdriven transition during period 1 between an initial voltage during period 0 and a final voltage during period 2. The signal 50 can be made from a combination of

15 a step function signal 52, shown in FIG. 7B, and a another step function signal 55, shown in FIG. 7C, that is a scaled, inverted and delayed function of the signal 52. In this example, the voltage change of signal 55 is a small fraction of that of signal 52, delayed by one period, which

20 may be equal to a bit signal duration.

FIG. 8 shows a device 100 that can provide the transition drive signals shown in FIG. 6 and FIG. 7. An encoder 102 receives binary MSB and binary LSB signals and converts pairs of those 2-PAM signals into digital input

25 signals along lines C1, C2 and C3 for a main driver 105 having three current sources 111, 112 and 113, to convert the binary data of the MSB and LSB into 4-PAM data at an output pad 115. The input signals on lines C1, C2 and C3 may be thought of as a thermometer code for the driver; the

30 more input signals on, the more current sources 111, 112 and 113 are activated.

Also receiving the input signals from encoder 102 is delay mechanism 118, which inverts and delays by one bit signal period the input signals to feed signals E1, E2 and E3 to auxiliary driver 120. Auxiliary driver current

5 sources 121, 122 and 123 are similar to respective main driver current sources 111, 112 and 113, but each auxiliary driver current source 121, 122 and 123 has a gain that is a fraction of respective main driver current sources 111, 112 and 113. Thus when main driver 105 outputs signal 52 of

10 FIG. 7B, auxiliary driver 120 outputs signal 55 of FIG. 7C, which is delayed, inverted and proportional to signal 52. The signals 52 and 55 combine at line 128 to form the desired signal 50 of FIG. 7A.

Referring again to FIG. 6, the main driver 105 can be

15 represented with the letter M and the auxiliary driver 120 with the letter S, with the numeral preceding each letter describing how many of the respective current sources are active. Thus FIG. 7B may represent the voltage driven by the main driver 105, which transitions from 3M to 0M at

20 T=1, and FIG. 7C may represent the voltage driven by the auxiliary driver 120, which transitions from 0S to 3S at T=2. A ratio of the gain of the auxiliary driver, S, to that of the main driver, M, is termed k, the equalization coefficient of the auxiliary driver. The ratio k is less

25 than one, and may range from about one percent to about fifty percent.

Although current sources 111, 112, 113, 121, 122 and 123 are shown as having a single transistor, each of these current sources may include multiple transistors that may

30 differ in power or number from the other current sources. The output voltages of the device 100 of FIG. 8 would have a distortion, for example, if each of the current sources

111, 112 and 113 were identical, since the drain to source voltage drop for each depends in part on whether the others are active, affecting the current. To compensate for this gds distortion the current sources can differ in number or transistor gain, e.g., by adjusting channel width. Current sources 111, 112, 113, 121, 122 and 123 may also receive additional input signals, for example, to adjust signal strength due to process, voltage and temperature (PVT) conditions. In addition, data may be transmitted at both rising and falling clock edges, so a pair of substantially identical main drivers and auxiliary drivers may exist for driving multi-PAM signals from input signals generated from MSB and LSB odd and even signals.

Auxiliary driver current sources 121, 122 and 123, which may also suffer from gds distortion unless adjusted as described above, drive much less current than the corresponding main driver current sources 111, 112 and 113. For example, each of main driver current sources 111, 112 and 113 may be formed of more current sources than respective auxiliary driver current sources 121, 122 and 123. Alternatively, main driver current sources 111, 112 and 113 may be formed of transistors having wider channels than those of respective auxiliary driver current sources 121, 122 and 123. Thus the output of auxiliary driver current sources 121, 122 and 123 are substantially proportional to the main driver current sources 111, 112 and 113.

In FIG. 9, the drivers 105 and 120 and delay element 118 are represented as a FIR filter 130. Input signals from the encoder are sent to the filter, which operates on the signals with function M and delays, inverts and

operates on the signals with function S, to output a filtered signal.

Equalization techniques similar to those described above for attenuation can be used to compensate for

5   crosstalk and reflection errors. FIG. 10 and FIG. 11 show a general system for filtering errors on a line V(N) using self equalization FIR 130 as described above and with crosstalk equalization FIR 133 and crosstalk equalization FIR 135 due to crosstalk from adjacent lines $A_1(N)$ through

10   $A_J(N)$, respectively, to produce equalized output V'(N). FIG. 11A shows a step function signal 150 in line A_1 that generates, as shown in FIG. 11B, a transient signal 152 in line V due to inductive coupling. FIG. 11C shows an equalization signal 155 that is generated by inputting

15   signal 150 to crosstalk equalization FIR 133 to compensate for transient signal 152. Capacitive crosstalk generated in line V from lines A_1 through A_J can be equalized in a similar fashion. Both inductive and capacitive crosstalk may generate a transient signal having a polarity dependent

20   upon the location of the receiver compared to the location at which the transient signal was generated. FIG. 11D shows a first signal component 160 that may be used to compensate for such an inductive or capacitive crosstalk error, which is a scaled and inverted function of signal

25   150 that generated the error. FIG. 11E shows a second signal component 162 that may be added to the signal 160 to create the crosstalk equalization signal 155 of FIG. 11C. Signal 162 can be scaled or fractional function of signal 150 that is delayed one bit period.

30   FIG. 12 shows a mechanism 200, connected with device 100 of FIG. 8, that can be used to equalize inductive or capacitive crosstalk errors created by signals in line 128

and felt in lines that are adjacent line 128, the adjacent
lines not shown in this figure. A first crosstalk
equalization driver 205 receives signals along lines P1, P2
and P3 that have been inverted by inverters 210,

5   controlling current sources 211, 212 and 213. The combined
current from those current sources 211, 212 and 213 is
output on a crosstalk equalization line 220 that is
connected to an adjacent line, not shown, the adjacent line
subjected to crosstalk errors from line 128. The output on

10   line 220 from driver 205 is thus scaled and inverted
compared to the signal produced by main driver 105, much
like signal 160 of FIG. 11D is a scaled and inverted
compared to signal 150 in FIG. 11A.

A second crosstalk equalization driver 225 receives

15   input signals along lines X1, X2 and X3 that have been
delayed by delay 110, lines X1, X2 and X3 controlling
current sources 221, 222 and 223. Thus the output of
second crosstalk equalization driver 225 on line 220 is
delayed and scaled compared to the signals produced by main

20   driver 105, much like signal 162 of FIG. 11E is scaled and
delayed compared to signal 150 in FIG. 11A. The combined
output of crosstalk equalization drivers 205 and 225 on
line 220 is much like signal 155 of FIG. 11C, which can be
used to compensate for transient signal 152 of FIG. 11B.

25   Thus crosstalk equalization drivers 205 and 225 can
compensate for crosstalk inflicted by line 128 on nearby
lines. An advantage of the circuit shown in FIG. 12 is
that cost and space effective circuits are implemented that
generate equalization signals by tapping into the input

30   signals for the main signal driver, instead of generating
equalizing signals based upon the output signals that are
transmitted.

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Similar equalization mechanisms can be used to compensate for reflections in a transmission line due to impedance discontinuities in the line. These reflections may be positive or negative, and may occur at various times

5   relative to the main signal. Thus for example a known reflection may occur at a receiver with a delay of two clock cycles, for which plural unit delay elements may be provided between the input signals and the compensation circuits. Moreover, although a 4-PAM signaling system is

10   shown, additional signal levels are possible with the provision of additional current sources. Unit delay elements may be provided for example by flip-flops, whereas delay elements that generate delays of less than a bit period may be provided for instance by inverters.

15   FIG. 13 shows another mechanism for equalizing multi-PAM signals, however the equalization mechanism inputs, on two lines, the MSB and LSB signals, rather than inputting the three lines of thermometer code inputs. A unit delay element 230 receiving the MSB and LSB outputs those signals

20   with a delay substantially equal to one signal bit duration. Unit delay 230 allows comparison at transition mapping device 233 of the MSB and LSB with the previous MSB and LSB, to gauge the multi-PAM transition between the prior and current MSB and LSB. Based upon this transition,

25   transition mapping device 233 outputs a three bit signal to current digital-analog converter (IDAC) 235, which drives a compensation signal on line 237, which in this example connects with a multi-PAM signal, not shown in this figure, to compensate for crosstalk on that other line.

30   FIG. 14 shows such a general equalization system that can be used to compensate for various signal imperfections, whether the imperfections are due to attenuation,

crosstalk, or reflections. Input signals on lines C(N) that control a main driver M(N) pass through a number J of delay elements D1 through DJ, each of which delay the input signals by one bit signal period. Various self-

5   equalization drivers S(N) through S(N+J), each of which is proportional to main driver M(N), are tapped off the input signals at various delay times. The equalization drivers S(N) through S(N+J) may each have a gain that is a different fraction of that of the main driver, and may or

10 may not invert the input signals, depending upon the particular equalization desired. The output of the main driver and each of the equalization drivers are then combined to produce equalized signal V'(N). Various crosstalk-equalization drivers X(N) through X(N+J), each of

15 which is proportional to main driver M(N), are also tapped off the input signals at various delay times, to provide crosstalk compensation signal X'(N) to an adjacent signal line.

FIG. 15 illustrates a mechanism 600 for adjusting

20 equalization parameters such as the magnitude, timing and sign of the equalization signal. An encoder 302 provides input signals on lines C(N) to a main signal driver, not shown in this figure, the input signals also encountering delay elements D1 and D2 that delay the input signals C(N)

25 by one unit delay each, to provide delayed signals on lines C(N+1) and C(N+2). Signals on lines C(N), C(N+1) and C(N+2) are input to multiplexers MUX 307 and MUX 308, which choose, based upon selection lines S1 and S2, which of input signals on lines C(N), C(N+1) and C(N+2) to input to

30 equalization drivers 310 and 320. As discussed, the equalization drivers may have different current gains. Exclusive OR gates 315 and 325 can be controlled to invert

or not to invert the input signals selected by multiplexers MUX1 and MUX2. This system can be expanded to provide multiple equalization drivers, XOR gates, multiplexers and delay elements, which together afford a variety of

5   combinations of scaling, timing and inversion of the input signals to produce a desired equalization.

FIG. 16 shows the encoder 102 that converts MSB and LSB signals into input signals that are output on lines C1, C2 and C3 to control the output driver 105. Data may be

10   transmitted and read at both rising and falling clock edges, so a pair of identical encoders may exist for translating MSB and LSB odd and even signals, with the encoders' output multiplexed on lines C1, C2 and C3. The MSB is input to a latch 352 that also receives a transmit

15   clock signal (TCLK) and complementary transmit clock signal (TCLK_B) for differentially latching the MSB as an input signal on line C2. The MSB is also input to an OR gate 340 that receives as the other input LSB. The output of OR gate 340 is latched at 350, which outputs another input

20   signal on line C1. The LSB passes through inverter 348 to become LSB_B, which is input to an AND gate 344 that receives as the other input the MSB. The output of AND gate 344 is clocked at 355 and output on line C3 as a third input signal.

25   Thus for MSB=0 and LSB=0, all the input signals are off. For MSB=0 and LSB=1, the OR gate 340 outputs on so that input signal C1 is on, but C2 and C3 are still off. When both MSB=1 and LSB=1, input signals C1 and C2 are on, but AND gate 344 inputs LSB_B, which is low so the input

30   signal on line C3 is off. When MSB=1 and LSB=0, input signals on all the lines C1, C2 and C3 are turned on. In this fashion the MSB and LSB may be combined as Gray code

and translated to thermometer code input signals on lines
C1, C2 and C3 that control the current sources to drive 4-
PAM signals.

FIG. 17 shows an integrating receiver 400 that may be
used to receive the multi-level signals sent by drivers
such as those described above, and decode the signals into
MSB and LSB components. As mentioned above, the data may
be transmitted at twice the clock frequency, and a pair of
receivers 400 may read even and odd data. An MSB receiver
402 of the 4-PAM receiver 400 in this example receives and
decodes a 4-PAM input signal VIN by determining whether the
signal VIN is greater or less than VREFM. In the MSB
receiver 402, a latching comparator 404 compares the value
of the voltage of the received input signal VIN to the
reference voltage VREFM and latches the value of the result
of the comparison B in response to a receive clock signal.
In one embodiment, data is taken at both rising and falling
clock edges. In an LSB receiver 408 two latching
comparators 410 and 414 compare the value of the voltage of
the received input signal VIN to the reference voltages
VREFH and VREFL, and latch the value of the result of the
comparison A and C, respectively, in response to the
receive clock signal. To decode the LSB, the signals from
the comparator outputs B, A, and C are then passed through
combinational logic 420. The latching comparators 404, 410
and 414 are implemented as integrating receivers to reduce
the sensitivity of the output signal to noise. This can be
accomplished by integrating a comparison of whether the
input signal is above or below the reference voltages over
most or all of the bit cycle, and then latching the
integrated result as the outputs A, B and C. Examples of

integrating receivers can be found in above-referenced U.S. Patent Application Serial Number 09/478,916.

Errors generated by crosstalk or capacitive coupling may be attenuated by the time they reach a receiver, which may in circuit board implementations be located up to about a foot away from the signal drivers, much as the transitions are attenuated over that distance. For crosstalk errors this attenuation may actually be beneficial as it tends to smooth out a high-frequency transient signal into a transient signal that may be compensated with an equalization having a duration of one bit. In a situation for which a neighbor's signal still has a high-frequency component when received, an integrating receiver can also smooth the data, so that compensating for a DC component of the crosstalk can be accomplished.

FIG. 18A shows a signal 450 undergoing a transition that may generate crosstalk in an adjacent line having a signal 452 shown in FIG. 18B. The crosstalk is apparent in FIG. 18B as a spike or high frequency component that is disturbing a step function transition. FIG. 18C shows an equalization signal 455 designed to compensate for a DC component of the spike of FIG. 18B. Combination of signal 452 and compensating signal 455 is shown in FIG. 18D as signal 457, which may leave a dipole component of the spike uncompensated. FIG. 18E shows that after integration by the receiver of FIG. 17 the dipole component has been removed, leaving a smooth transition signal 459.

As illustrated in FIG. 19, in a system that has numerous closely spaced signal lines S1, S2, S3 and S4, such as a bus for a computer or similar device, crosstalk may exist between each line and each nearby line. This

crosstalk may have characteristics, based upon how many
lines are between the crosstalk creator and the crosstalk
victim, which can be equalized with an FIR having
corresponding equalization characteristics, such as
5   magnitude, timing and sign. Since these crosstalk
characteristics have a regular pattern, crosstalk FIRs for
each line may have a number of standard equalization
drivers each designed to compensate for crosstalk a certain
number of lines away. Thus self FIR 500, self FIR 502,
10   self FIR 505 and self FIR 508 may each have equal ratios k
which can be used to compensate for attenuation and
reflections. Similarly XTK 510, XTK FIR 512, XTK FIR 515
and XTK FIR 518 may each have equal ratios k' that depend
upon whether a line being equalized is a first adjacent
15   line, second adjacent line, third adjacent line or further
spaced from the crosstalk generating and equalizing line.

        As shown in FIG. 20 spaced signal lines S1, S2, S3 and
S4 may be grouped in pairs or other arrangements, for
example with a ground wire disposed between the pairs of
20   lines. In this case, crosstalk equalization FIRs 560, 562,
565 and 568 may distinguish whether a signal line subjected
to crosstalk from and adjacent signal line is spaced apart
by a ground wire, and adjust the equalization parameters
accordingly. Similarly, lines that are adjacent in one
25   area, such as at signal pads for a circuit, may be
separated in another area, for example due to routing in
separate layers of a circuit board. In this situation,
alternately spaced lines, such as S1 and S3, may induce
more crosstalk in each other than adjacent lines, such as
30   S1 and S2, and the equalization parameters may be adjusted
accordingly.

FIG. 21 illustrates a memory system 600 in which embodiments of the present invention may be applied. The system 600 includes a printed circuit board 601 (sometimes called a motherboard) to which a memory controller 603, a

5　signaling path 605 and connectors 607A, 607B are affixed. Memory modules 609A, 609B, each containing one or more memory devices 611, are affixed to the printed circuit board 601 by being removably inserted into the connectors 607A, 607B. Though not shown in FIG. 21, the memory

10　modules 609A, 609B include traces to couple the memory devices 611 to the signaling path 605 and ultimately to the memory controller 603.

In the embodiment of FIG. 21, the signaling path 605 constitutes a multi-drop bus that is coupled to each memory

15　module. The individual memory devices of a given module may be coupled to the same set of signaling lines within signaling path 605, or each memory device of the module may be coupled to a respective subset of the signaling lines. In the latter case, two or more memory devices 611 on a

20　module may be accessed simultaneously to read or write a data value that is wider (i.e., contains more bits) than the data interface of a single memory device. In an alternative embodiment (not shown), each of the memory modules may be coupled to the memory controller via a

25　dedicated signaling path (i.e., a point-to-point connection rather than a multi-drop bus). In such an embodiment, each of the memory devices on the memory module may be coupled to a shared set of signaling lines of the dedicated path, or each memory device may be coupled to respective subsets

30　of the signaling lines.

The signaling path 605 may include a single, multiplexed set of signal lines to transfer both data and

control information between the memory controller 603 and memory devices 611. Alternatively, the signaling path 605 may include a set of signaling lines for transferring data between the memory devices 611 and the memory controller

5   603, and a separate set of signaling lines for transferring timing and control information between the memory devices 611 and the memory controller 603 (e.g., clock signals, read/write commands, and address information). Preferably the control information is uni-directional, flowing from

10   the memory controller 603 to the memory devices 611, but status information may also be communicated from the memory devices 611 to the memory controller. Also, the timing information may be generated within the memory controller 611, or by external circuitry (not shown).

15   In one embodiment, selected signaling lines within signaling path 605 are used to carry multi-level signals (e.g., 4-PAM signals) between the memory devices 611 and the memory controller 603. For transfers from the memory controller 603 to a given memory device 611, a set of

20   driver circuits within the memory controller 603 output multi-level signals onto the selected traces of the signaling path, with equalization and/or cross-talk cancellation being applied to each such signal as described above. Receiver circuits within the addressed memory

25   device (or memory devices) receive the multi-level signals from the memory controller 603 and convert the signals into corresponding binary representations. Conversely, for transfers from the memory device 611 to memory controller 603 (e.g., in response to a read command issued to the

30   memory device 611 by the memory controller 603), driver circuits within the memory device 611 output equalized and cross-talk-canceled multi-level signals onto the selected

set of traces of the signaling path for receipt by receiver circuits within the memory controller 603. Such multi-level signaling may be used to transfer both data and control information between the memory controller 603 and

5 the memory devices 611, or multi-level signaling may be used for one type of information transfer (e.g., data or control), but not the other. Further, the signaling technique used to transfer either data or control information (or both) may be dynamically switched between

10 binary and multi-level signaling according to detected events, such as bandwidth demand, detection of a threshold error rate, and so forth.

Although a memory system that includes connectors for removable insertion of memory modules is depicted in FIG.

15 21, other system topologies may be used. For example, the memory devices need not be disposed on memory modules, but rather may be individually coupled to the printed circuit board 601. Also, the memory devices, the memory controller and the signaling path may all be included within a single

20 integrated circuit along with other circuitry (e.g., graphics control circuitry, digital signal processing circuitry, general purpose processing circuitry, etc.). The system of FIG. 21 can be used in any number of electronic devices, including without limitation, computer

25 systems, telephones, network devices (e.g., switch, router, interface card, etc.), handheld electronic devices, intelligent appliances.

Although we have focused on teaching the preferred embodiments of a low latency multi-line, multi-level

30 equalized communication system, other embodiments and modifications of this invention will be apparent to persons of ordinary skill in the art in view of these teachings.

Therefore, this invention is limited only by the following claims, which include all such embodiments, modifications and equivalents when viewed in conjunction with the above specification and accompanying drawings.